ABSTRACT OF THE DISCLOSURE

There are many inventions described and illustrated herein. In a first aspect, the present invention is directed to a memory device and technique of reading data from and writing data into memory cells of the memory device. In this regard, in one embodiment of this aspect of the invention, the memory device and technique for operating that device that minimizes, reduces and/or eliminates the debilitating affects of the charge pumping phenomenon. This embodiment of the present invention employs control signals that minimize, reduce and/or eliminate transitions of the amplitudes and/or polarities. In another embodiment, the present invention is a semiconductor memory device including a memory array comprising a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns. Each semiconductor dynamic random access memory cell includes a transistor having a source region, a drain region, a electrically floating body region disposed between and adjacent to the source region and the drain region, and a gate spaced apart from, and capacitively coupled to, the body region. Each transistor includes a first state representative of a first charge in the body region, and a second data state representative of a second charge in the body region. Further, each row of semiconductor dynamic random access memory cells includes an associated source line which is connected to only the semiconductor dynamic random access memory cells of the associated row.